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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,927	06/27/2000	YASUTAKA NAKASHIBA	186709/99	3707

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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,927	NAKASHIBA, YASUTAKA	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/27/2005 & 7/26/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/27/2005 & 7/26/2005 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 7/26/2005 was filed after the mailing date of the Final Office Action on 1/25/2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The drawings were received on 6/27/2005. These drawings are Figures 12-15.

Response to Arguments

4. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

5. Claims 15, 16 & 19 are objected to because of the following reasons:

Regarding claim 15, the last limitation of claim 15 recites, "said light shielding film." There is insufficient antecedent basis for this limitation in the claim. This is suggested to be changed to --said first light shielding layer--.

Regarding claim 16, recitation of "said image signal part" also lacks antecedent basis, and is suggested to be changed to --said image sensor part--.

Regarding claim 19, a comma should be placed before the word "wherein" in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 6,043,115) in view of Tanaka Nagataka (JP 11-097662).

Regarding claim 1, Pan discloses a solid-state image pickup device comprising:

a multilevel wiring structure including a first group of wirings (216) at a first level and a second group of wirings (222) at a second level, said first level being closer to a semiconductor substrate (200) than said second level (see Fig. 2E; col. 3, lines 4-32);

a photoelectric conversion part (204) on said semiconductor substrate, said photoelectric conversion part having a photoelectric conversion region (also 204 under microlens 230) as shown in Fig. 2E, col. 3, lines 34-44;

a logic circuit part (CMOS transistors formed by source/drain 204/206 regions and gate 202 regions) on said semiconductor substrate, said logic circuit part including a plurality of transistors (CMOS transistors mentioned above) to manipulate an electrical signal produced from said photoelectric conversion part and having a first wiring (216) formed at said first level (see Fig. 2E and col. 2, lines 54-59);

a light shielding film (**inter-metal** layer 218) defining a region (opening 226) of beam incidence on said photoelectric conversion region (see Fig. 2E; col. 3, lines 10-11 and col. 3, lines 23-26, wherein inter-metal layer 218 is a thin layer made of metal that constitutes a light shielding film);

Pan is silent about a light shielding layer (another shielding layer) covering said logic circuit part, wherein light shielding film is formed at said first level and provided at a height closer to said semiconductor substrate than said light shielding layer.

Nagataka teaches an image sensor having a multilevel wiring structure (Fig. 9), wherein **a second** light shielding layer (aluminum layer 110) is provided at the topmost layer under transparent layer 108 but over a first light shielding layer (106, 107 shown in Fig. 6) for covering wirings of manipulation transistors 32, 33 (Fig. 2) to prevent the transistors terminal from exposing to light that would cause circuit malfunctioning . See Figs. 2 & 9 and paragraphs [0028] – [0031].

Therefore, it would have been obvious to one of ordinary skill in the art to provide a second light shielding layer at a substantial top layer of the image pickup device in which the second light shielding layer is farther to the semiconductor substrate than the first light shielding layer (which is closer to the semiconductor substrate) so as to effectively cover manipulation transistors from incident light to avoid circuit malfunctioning.

Regarding claim 2, the combination of Pan and Nagataka also teaches that said light shielding film (218 in Pan) is located position between said light shielding layer (top layer 110 in Nagataka) and said photoelectric conversion region in the direction of beam incidence. See Fig. 2E in Pan and Fig. 9 in Nagataka as analyzed in claim 1.

Regarding claim 3, it is also seen from Fig. 2E in Pan that the light shielding film (218) is provided so as to cover (at least partially cover) said photoelectric conversion part (204) as well as to make the light shielding state continuous in the boundary part between said photoelectric conversion part and said logic circuit part.

Regarding claim 4, the combination of Pan and Nagataka also teaches that the light shielding film and the light shielding layer are connected in such a manner to make the light shielding state continuous in said boundary part. See the analysis of claim 1, Fig. 2E in Pan and Fig. 9 in Nagataka, wherein the shielding film 218 and shielding layer 110 are overlapped toward the boundary part.

Regarding claim 5, see the analysis of claim 4.

Regarding claim 6, Pan in view of Nagataka further teaches that the light shielding film covers the photoelectric conversion part by combining a plurality of layers. See Fig. 2E in Pan, wherein at least 3 layers of 224, 218 and 212 constitutes a plurality layers, or Figs. 6 & 9 in Nagataka, [0028] – [0031].

Regarding claims 7-10, see the analyses of claims 1 & 6.

Regarding claim 8, Pan in view of Nagataka further teaches that a plurality of light shielding films are provided so as to make the light shielding state continuous in their boundary parts. See Nagataka, Figs. 6 & 9, [0028] – [0031].

Regarding claim 11, it is clear in Nagataka that the light shielding layer is formed of a material (aluminum layer 110) that has either low light transparency or high light absorbency such that its light shielding property is high. See [0031].

Regarding claim 12, the light shielding film in Pan is made in a CMOS process during the manufacturing of the CMOS image sensor including CMOS transistors (see col. 1, lines 5-10). Thus, the process is the same CMOS process.

Regarding claim 13, see the analysis of claim 1.

Regarding claim 14, it is clear in Pan that the image pickup device is a CMOS sensor (see Pan, col. 1, lines 5-10.

7. Claims 15 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,172,351 B1) in view of Pan (US 6,043,115).

Regarding claim 15, Kimura discloses a solid-image pickup device comprising:

an image sensor part (image pickup portion 12) producing an analog signal in response to incident light to said image sensor part (see Figs. 2, 5 & 6; col. 2, line 52 – col. 3, line 12);

a first circuit part (A/D converter 13c) producing a digital signal in response to said analog signal (see Fig. 2; col. 2, line 62);

a second circuit part (signal processing portion 13d) performing signal processing on said digital signal (see Fig. 2; col. 2, line 63);

said image sensor part (12) and said first (13c) and second (13d) circuit parts being formed on a semiconductor substrate (substrate 11 of image sensor chip) as shown in Figs. 2, 5 & 6; col. 2, line 52 – col. 3, line 12;

a first wiring provided in at least one of said first and second circuit parts (see Fig. 2, wherein circuit wirings for A/D converter and signal processing portion are inherent for the image pickup device to function as disclosed).

a second light shielding layer (TAB tape 17 and/or black film 61 shown in Figs. 4 & 6) covering said first and second parts (see col. 3, lines 13-19 and col. 4, lines 26-34).

Although Kimura discloses a fully integrated image pickup device on a single semiconductor substrate (IC 11) having all limitations analyzed above including a "second" light shielding layer (17 or 61) that is built on top of the IC 11, Kimura does not specifically teach in detail that the image pickup device comprises a multilevel wiring structure on a semiconductor substrate, a first and second levels of a wiring layer provided in said multilevel wiring structure, said first level being closer to said semiconductor substrate that said second level, a first light shielding layer covering said image sensor part (light shielding layer for each pixel in image sensor portion 12), said first light shielding layer is provided closer to said semiconductor substrate than said second light shielding layer, and said first wiring and said light shielding film (understood as said first light shielding layer to meet antecedent basis) are provided in said first level.

Pan teaches a solid-image sensor in *detailed layout* that includes a multilevel wiring structure (Fig. 2E) on a semiconductor substrate (200), first and second levels (216 & 222) of a wiring layer is provided in the multilevel wiring structure, the first level (216) is closer to the semiconductor substrate (200) than the second level (222), a first shielding layer (formed by inter-metal layer 218) covers the image sensor part (204, 202, 206). See Fig. 2E and col. 2, line 50 – col. 3, line 44. Pan also clearly shows that the first light shielding layer (218) is provided close to the semiconductor substrate and that the first wiring and said first light shielding layer (218) are provided in said first level (Fig. 2E). Such arrangement for the multilevel wiring structure would reduce size of image sensor and prevent interference in the image sensor (see Pan; col. 2, lines 10-30).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kimura and Pan to arrive at the Applicant's claimed invention so as to reduce image sensor size and prevent interference in the image sensor.

It should be noted that the shielding layer 17 or 61 in Kimura is always farther from the substrate than the light shielding layer 218 of the image sensor in Pan (this is corresponding to image pickup portion 12 in Kimura).

Regarding claim 16, it is clear in Pan that the image [sensor] part includes a photoelectric conversion region (204) generating electrical charge in response to said light and a transistor (formed by source/drain 204/206 and gate 202) producing said analog signal in response to said electrical charge. See Pan, col. 2, line 50 – col. 3, line 44.

Allowable Subject Matter

8. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 17 & 18, the prior art of record fails to teach or fairly suggest, in combination with their corresponding independent claims, the limitation "*a second wiring provided in said photoelectric conversion part, wherein said second wiring and said light shielding layer are provided in said second level.*"

Regarding claim 19, the prior art of record also fails to teach or fairly suggest, in combination with the corresponding independent claim, the limitation "*a second wiring provided in said image sensor part, wherein said second wiring and said light shielding layer are provided in said second level.*"

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 7:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER